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| **Code of Institute:** |  |
| **Branch:** | ETRX |
| **Sem:** | VIII |
| **Subject Name (with Subject Code):** | **Analog and Mixed VLSI Design**  **(ELX802)** |
| **Number of questions:** | **110** |

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| **Type** | **Low level (LL) (2mark each)** |
|  | The voltage generated according to \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ is called a bandgap reference  a. VREF = VCE + VT *ln*n  b. VREF = VBE + VT *ln*n  c. VREF = VBE + VG *ln*n  d. VREF = VBE + VD *ln*n |
| Answer: Option b. VREF = VBE + VT *ln*n |
|  | Which of the following statement regarding MOSFET is not true?  a. Easily scalable  b. Low fabrication cost  c. High power dissipation  d. Possible of placing both analog & digital circuits on the same chip. |
| Answer: Option c. High power dissipation |
| 3. | According to the principle of current mirror, if gate-source potentials of two identical MOS transistors are equal, then the channel currents should be \_\_\_\_\_\_\_  a. Iref - Io  b. Iref = Io  c. Iref > Io  d. Iref < Io |
| Answer: Option b) Iref = Io |
| 4 | Which of the following is not name of fourth terminal of MOSFET?  a. substrate  b. bulk  c. body  d. base |
| Answer: Option d. base |
| 5 | A MOSFETs may be used as a switching device or as a\_\_\_\_\_\_\_\_\_\_\_\_\_  a. Tuning device  b. Rectifier  c. Inductor  d. Variable resistor |
| Answer: Option d. Variable resistor |
| 6. | Which of the following is the equation for output current in current mirror circuit?  a. Iout = (W/L)2/ (W/L)1 IREF  b. Iout = (W/L)1/ (W/L)2 IREF  c. IREF = (W/L)2/ (W/L)1 Iout  d. Iout = (L/W)2/ (W/L)1 IREF |
| Answer: Option a. Iout = (W/L)2/ (W/L)1 IREe |
| 7. | In addition to supply, process, and temperature variability, several other parameters of reference  generators may be critical as well. These include \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.  a. input impedance, gain, and power dissipation  b. output impedance, output noise, and power dissipation  c. output impedance, slew rate, and power dissipation  d. output impedance, speed, and linearity |
| Answer: Option: b. output impedance, output noise, and power dissipation |
| 8 | The 4 terminals of MOSFET are\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.  a. Drain, Source, Gate, substrate  b. Drain, Source, Gate, emitter  c. Drain, Source, Gate, collector  d. Drain, Source, Gate, base |
|  | Answer: Option a. Drain, Source, Gate, substrate |
| 9 | Which important mechanism is connected to the drives the circuit out of the degenerate bias point when the supply is turned on?  a. diode-connected device NMOS M5  b. capacitor at drain terminal of device M1  c. resistor-connected device PMOS M5  d. addition of resistor at drain terminal of NMOS M2 |
|  | Answer: Option a. diode-connected device NMOS M5 |
| 10 | For obtaining a reference voltage, select appropriate equation, with zero TC.  a. VREF = α1V1 + α2V2.  b. VREF = α1V1 - α2V2  c. VREF = α1V1 \* α2V2  d. VREF = α1V1/ α2V2 |
|  | Answer: Options a. VREF = α1V1 + α2V2 |
| 11 | If two identical transistors (IS1 = IS2) are biased at collector currents of nI0 and I0 and their base currents are negligible, then  a. ∆VBE = VBE1 − VBE2  b. ∆VBE = VBE1 + VBE2  c. ∆VBE = VBE1 x VBE2  d. ∆VBE = VBE1 / VBE2 |
|  | Answer: Options a. ∆VBE = VBE1 − VBE2 |
| **12** | In the given equation Vout = VBE2 + (VT *ln*n) (1 + R2/R3), for a zero TC, we must have (1 + R2/R3) *ln* n ≈ 17.2 and R2/R3 = 4, then we may choose  a. n = 30  b. n = 31  c. n = 32  d. n = 33 |
|  | Answer: Options b. n = 31 |
| **13** | Bandgap Reference, VREF ≈ VBE + 17.2VT  a.≈ 1.35 V  b.≈ 1.25 V  c.≈ 1.15 V  d.≈ 1.45 V |
|  | Answer: Options d) d.≈ 1.45 V |
| **14** | How must n be chosen to yield a TC of +1.5 mV/K so as to cancel the TC of the base-emitter voltage at T = 300 K?  a. n = 1.95 × 107  b. n = 2.95 × 105  c. n = 2.95 × 107  d. n = 2.95 × 106 |
|  | Answer: Options b. n = 2.95 × 107 |
| **15** | Referring to the equation, VREF = Eg/q + (4 + m) VT, the term “bandgap” is used here because as \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.  a. T →0, VREF → Eg/q  b. VREF →0, T→ Eg/q  c. T →0, VREF → (4 + m) VT  d. T →0, VREF → Eg/q |
|  | Answer: Options a. T →0, VREF → Eg/q |
| **16** | In idea of circuit of Constant-Gm biasing by means of a switched-capacitor “resistor” is to establish an \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_between the source of M2 and ground, where fCK denotes the clock frequency.  a. average capacitance equal to (CSfCK)−1  b. average frequency equal to (CSfCK)−1  c. average transconductance equal to (CSfCK)−1  d. average resistance equal to (CSfCK)−1 |
|  | Answer: Option d. average resistance equal to (CSfCK)−1 |
| **17** | This Analog multiplier is termed as four-quadrant multiplier because \_-  a. both inputs can be either positive or negative around a common-mode voltage, VCM  b. both inputs can be positive around a common-mode voltage, VCM  c. both inputs can be negative around a common-mode voltage, VCM  d. only one input can be either positive or negative around a common-mode voltage, VCM |
|  | Answer: Option a. both inputs can be either positive or negative around a common-mode voltage, VCM |
| **18** | The Differential output of the difference amplifier is the amplification of \_\_\_\_\_\_\_\_\_\_  a) Difference between the voltages of input signals  b) Difference between the output of the each transistor  c) Difference between the supply and the output of the each transistor  d) Addition between the output of the each transistor |
|  | Answer: Option (a) Difference between the voltages of input signals |
| **19** | DNL stands for   1. Differential Nonexistenc 2. Displacement nonlinearity 3. Dominant Nonlinearity 4. Differential Nonlinearity |
|  | Answer: Option d) Differential Nonlinearity |
| **20** | The center potential in differential signaling is called  a) The differential mode level  b) The common mode level  c) CMRR  d) Slew rate |
|  | **Answer: Option**  **(a)**  The common mode level |
| **21** | Thermal noise current in the MOSFET is proportional to:  a) Transconductance  b) Resistance  c) Gate voltage  d) drain voltage |
|  | Answer: Option (a) Transconductance |
| **22** | The noise temperature at a resistor depends upon   1. Resistance value 2. Noise power 3. noise bandwidth 4. d. noise voltage |
|  | **Solution (b)**  Noise power |
| **23** | Which of the following is true |
|  | **Answer: Option (b )** |
| **24** | Which of the following is true |
|  | **Solution (a)** |
| **25** | Increasing Vsb \_\_\_\_\_\_\_ the threshold voltage.  a) does not effect  b) decreases  c) increases  d) exponentially increases |
|  | **Answer: Option ©** **increases** |
| **26** | Small signal differential voltage gain for the differential pair in equilibrium condition is given as |
|  | Solution (a) |
| **27** | **The common mode gain of differential amplifier is** |
|  | Answer: Option (a) |
| **28** | **The voltage gain of Differential amplifier with PMOS diode connected load is nearly equal to** |
|  | Answer: Option (b) |
| **29** | The voltage gain of Differential amplifier with current source load is nearly equal to |
|  | Answer: Option (b). |
| **30** | Noise voltage Vn and absolute temperature T are related as  **a.** Vn = 1/ √(4RKTB) **b.** Vn = √(4RK)/ (TB) **c.** Vn = √(4RKTB) **d.** Vn = √(4KTB)/R |
|  | **Answer: Option (c).** Vn = √(4RKTB) |
| **31** | In probability Noise is described as:  a) Random function  b) Random process  c) Deterministic function  d) Deterministic process |
|  | **Answer: Option (b)** Random process |
| **32** | The average power of flicker noise depends on:  a) Thickness of oxide  b) Cleanness of the oxide silicon interface  c) Voltage on oxide  d) Length of channel |
|  | **Answer: Option (b)** Cleanness of the oxide silicon interface |
| **33** | Find the voltage gain of the circuit assuming γ and λ=0.M1 and M2 MOSFETS connected in series and resistance RD is connected at Drain of M1 and input is applied to the gate of M1,M2 is PMOS connected to source of M1.Find the gain of the circuit. |
|  | **Answer: Option (C)** |
| **34** | The gain of CS stage with diode connected load with negligible channel length modulation (M1is driver andM2 is diode connected NMOS device ) is |
|  | **Answer: Option (a)** |
| **35** | In CS amplifier, constant current source of I1 is connected as load assume driver M1is in saturation region. What is gain of this configuration   1. 2 |
|  | **Answer: Option (a )** |
| **36** | The voltage gain of source follower is |
|  | **Answer: Option (a)** |
| 37 | The gain of Common Gate amplifier is   1. η)RD 2. η)RD 3. η)RD 4. η)RD |
| **Answer: Option (b)** η)RD |
| 38 | The gain of CS amplifier with PMOS diode connected load (M1is nmos and M2is pmos) is |
|  | Answer: Option (a) |
| 39 | In CS amplifier , noise voltage due to Rd at the output is   1. proportional to 2. proportional to 3. proportional to rd 4. proportional to |
| Answer: Option (a) proportional to |
| 40 | If an NMOS is degenerated by a resistor in series with the source, what will happen to the output resistance?  a) It increases  b) It decreases  c) It remains same  d) Cannot be determined |
| Answer: Option (a)It increases |
| 41 | |  | | --- | | For a pole frequency ω, the phase experiences a change of \_\_\_\_\_\_ at ω and for a zero frequency ω, the phase experiences a change of \_\_\_\_\_\_ at ω. | | 1. +45 deg/dec, -45 deg/dec | | 1. -45 deg/dec, +45 deg/dec | | 1. +90 deg/dec, -90 deg/dec | | 1. -90 deg/dec, +90 deg/dec | |
| Answer: Option : (b)-45 deg/dec, +45 deg/dec |
| 42 | Find out the the resolution of of 8 bit DAC/ADC?  a) 562  b) 625  c) 256  d) 265 |
|  | Answer: Option : (c) 256 |
| 43 | ADC conversion involves   1. Quantization 2. Simulation 3. Summation 4. Subtraction. |
|  | Answer: Option : (a) Quantization |
| 44 | ADC input is sampled by   1. Nyquist rate. 2. Newton rate 3. Ohms rate. 4. Lens rate |
|  | Answer: Option : (a) Nyquist rate |
| 45 | How to overcome the limitation of binary weighted resistor type DAC?   1. Using R-2R ladder type DAC 2. Multiplying DACs 3. Using monolithic DAC 4. Using hybrid DAC |
|  | Answer: Option : (a) Using R-2R ladder type DAC |
| 46 | The smallest resistor in a 12-bit weighted resistor DAC is 2.5kΩ, what will be the largest resistor value?   1. 40.96MΩ 2. 10.24MΩ 3. 61.44 MΩ 4. 18.43MΩ |
|  | Answer: Option : (b) 10.24MΩ |
| 47 | What is the disadvantage of binary weighted type DAC?   1. Require wide range of resistors. 2. High operating frequency 3. High power consumption 4. Slow switching. |
|  | Answer: Option : (a) Require wide range of resistors |
| 48 | Why the switches used in weighted resistor DAC are of single pole double throw (SPDT) type?   1. To connect the resistance to reference voltage 2. To connect the resistance to ground 3. To connect the resistance to either reference voltage or ground 4. To connect the resistance to output. |
|  | Answer: Option : (c) To connect the resistance to either reference voltage or groun |
| 49 | In a D-A converter with binary weighted resistor, a desired step size can be obtained by   1. Selecting proper value of VFS 2. Selecting proper value of R. 3. Selecting proper value of RF. 4. Selecting proper value of VS, |
|  | Answer: Option : (c) Selecting proper value of RF |
| 50 | Determine the Full-scale output in a 8-bit DAC for 0-15v range?   1. Full scale output=15.1v 2. Full scale output=15.2v 3. Full scale output=14.5v 4. Full scale output=14.94v |
|  | Answer: Option : (d) Full scale output=14.94v |
| 51 | |  | | --- | | Which of the following is called as Desensitivity factor. | | 1. 1+Aoβ | | 1. 1/ (1+Aoβ) | | 1. Ao/(1+Aoβ) | | 1. Ao \* (1+Aoβ) | |
|  | Answer: Option :a )1+Aoβ |
| 52 | |  | | --- | | An ideal op-amp has \_\_\_\_\_\_\_\_ | | 1. Zero input resistance | | 1. Zero differential voltage gain | | 1. Infinite output resistance | | 1. Infinite CMRR | |
|  | Answer: Option :c) Infinite output resistance |
| 53 | |  | | --- | | After Negative feedback the New pole ωf is placed at \_\_\_\_\_\_, Where Am is mid band Gain and ωo is initial dominant pole. | | 1. ωo/(1+Amβ) | | 1. ωo/( ωo +Amβ) | | 1. ωo×(1+Amβ) | | 1. ωo×( ωo +Amβ) | |
|  | Answer: Option c) ωo×(1+Amβ) |
| 54 | |  | | --- | | Closed loop gain of Amplifier is given by \_\_\_\_\_. | | 1. 1+Aoβ | | 1. 1/ (1+Aoβ) | | 1. Ao/(1+Aoβ) | | 1. Ao \* (1+Aoβ) | |
|  | Answer: Option c) Ao/(1+Aoβ) |
| 55 | |  | | --- | | The Barkhausen criterion for sustained Oscillation is \_\_\_\_\_. | | 1. IAβI=1, LAβ = 360 deg | | 1. IAβI ≠1, LAβ = 180 deg | | 1. IAβI<1, LAβ = 180 deg | | 1. IAβI>1, LAβ = 360 deg | |
|  | Answer: Option a) IAβI=1, LAβ = 360 deg |
| 56 | |  | | --- | | A single pole system cannot contribute a phase shift \_\_\_\_\_\_. | | 1. Greater than 180 deg | | 1. Less than 180 deg | | 1. Greater than 90 deg | | 1. Less than 90 deg | |
|  | Answer: Option c) Greater than 90 deg |
| 57 | |  | | --- | | The slope of the magnitude plot changes by \_\_\_\_\_ at every zero frequency and \_\_\_\_\_at every pole frequency | | 1. +40 dB/dec, -20 dB/dec | | 1. +20 dB/dec, -40 dB/dec | | 1. +20 dB/dec, -20 dB/dec | | 1. -20 dB/dec, +20 dB/dec | |
|  | Answer: Optionc)+20 dB/dec, -20 dB/dec |
| 58 | |  | | --- | | If P1, P2 are input, output poles before Miller compensation and P1’, P2’ are poles after compensation then \_\_\_\_\_ is true. | | 1. |p1| > |p1’| and |p2| < |p2’| | | 1. |p1| < |p1’| and |p2| > |p2’| | | 1. |p1| > |p1’| and |p2| > |p2’| | | 1. |p1| < |p1’| and |p2| < |p2’| | |
|  | Answer: Option a)|p1| > |p1’| and |p2| < |p2’| |
| 59 | |  | | --- | | The output impedance provided by Gain boosted cascode amplifier of transistors M1, M2 and amplifier A1 is given by \_\_\_\_\_\_. (where M1 is CS device, M2 is CG device and OPAMP A1 is gain boosting device) | | 1. Rout= gm1ro1 | | 1. Rout= A1gm2ro2ro1 | | 1. Rout= gm2ro2 | | 1. Rout= A1gm1ro2ro1 | |
|  | Answer: Option b) Rout= A1gm2ro2ro1 |
| 60 | |  | | --- | | Define the common-mode rejection ratio (CMRR) of op-amp? | | 1. CMRR=Ad/ACM | | 1. CMRR=ACM/ Ad | | 1. CMRR=VOCM/ACM | | 1. CMRR=Ad\*ACM | |
|  | Answer: Option a) CMRR=Ad/ACM |
| 61 | |  | | --- | | Common mode voltage gain of practical op-amp is generally \_\_\_\_\_\_\_. | | 1. >1 | | 1. =1 | | 1. <1 | | 1. =0 | |
|  | Answer: Option c) <1 |
| 62 | |  | | --- | | How the slew rate is represented? | | 1. 1V/ms | | 1. 1V/s | | 1. 1V/µs | | 1. 1mv/S | |
|  | Answer: Option c)1V/µs |
| 63 | |  | | --- | | Why the gain magnitude in frequency response plot is expressed in decibels (dB) | | 1. To obtain gain > 105 | | 1. To obtain gain < 105 | | 1. To obtain gain = 0 | | 1. To obtain gain = ∞ | |
|  | Answer: Option a) To obtain gain > 105 |
| 64. | If the input of type 1 PLL is a frequency step of Δw at t = 0, the change in phase at t = infinity is:  (a Δw (b) Δw/Kpd (c )  Δw/Kpd.Kvco (d)  Δw/Kvco |
| Answer: Option c)  Δw/Kpd.Kvco |
| 65 | Neglecting Channel Length Modulation, if the transconductance increases, the input impedance of a source follower stage \_\_\_\_\_\_\_\_\_\_\_  a) Remains the same  b) Increases  c) Decreases  d) Doubles |
| Answer: Option a) Remains the same |
| 66 | What is true for Phase frequency detector:  a) The output of the PFD does not depend on both the phase and frequency of the inputs.  b) The PFD will lock on a harmonic of the data.  c) A rising edge from the dclock and data must be present when doing a phase comparison  d) The outputs (Up and Down) of the PFD are both logic high when the loop is in lock |
| Answer: Option c) A rising edge from the dclock and data must be present when doing a phase comparison |
| 67 | The oscillation frequency for ring oscillator is \_\_\_\_\_\_\_\_.  a) Fosc= 1/n(tphl +tplh)  b) Fosc= (tphl +tplh)  c) Fosc= 1/n(tphl)  d) Fosc= 1/(tphl +tplh |
| Answer: Option a) Fosc= 1/n(tphl +tplh) |
| 68 | The gain of the voltage-controlled oscillator is \_\_\_\_\_\_\_.  a) Kvco = 2pi.(fmax -fmin)/ (Vmax-Vmin)  b) K vco =(fmax -fmin)/ (Vmax-Vmin)  c) K vco = 2.(fmax -fmin)/ (Vmax-Vmin)  d) K vco = 2pi.(fmax -fmin) |
| Answer: Option a) Kvco = 2pi.(fmax -fmin)/ (Vmax-Vmin) |
| 69 | |  | | --- | | Gain of the Phase detector for XOR PD is given by: | | 1. Kpd= VDD/π | | 1. Kpd= VDD | | 1. Kpd= 2VDD/π | | 1. Kpd= VDD/2π | |
|  | Answer: Option a) VDD/π |
| 70 | The gain of the voltage-controlled oscillator is \_\_\_\_\_\_\_.  a) Kvco = 2pi.(fmax -fmin)/ (Vmax-Vmin)  b) K vco =(fmax -fmin)/ (Vmax-Vmin)  c) K vco = 2.(fmax -fmin)/ (Vmax-Vmin)  d) K vco = 2pi.(fmax -fmin) |
|  | Answer: Option |
| 71 | |  | | --- | | System on chip means: \_\_\_\_\_\_\_ | | 1. It consists of both analog and digital IC | | 1. Analog IC | | 1. Digital IC | | 1. Discrete components | |
|  | Answer: Option a) It consists of both analog and digital IC |
| 72 | |  | | --- | | Which Hardware description language is used for ASICs? | | 1. Verilog | | 1. C | | 1. Oopm | | 1. Fortran | |
|  | Answer: Option a) Verilog |
| 73 | |  | | --- | | The closed loop gain of a working oscillator circuit is: | | 1. Less than 1. | | 1. More than 1 | | 1. Exactly 1 | | 1. Infinity | |
|  | Answer: Option c) Exactly 1 |
| 74 | |  | | --- | | If the input of type 1 PLL is a frequency step of Δw at t = 0, the change in phase at t = infinity is: | | 1. Δw | | 1. Δw/Kpd | | 1. Δw/Kpd.Kvco | | 1. Δw/Kvco | |
|  | Answer: Option c) Δw/Kpd.Kvco |
| 75 | |  | | --- | | In the circuit of figure, continuous-time feedback amplifier, the closed-loop gain is set by the ratio of R2 and R1, in order to avoid reducing the open-loop gain of the op amp, we postulate that the resistors can be replaced by \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_. | | 1. Inductors | | 1. Transistors | | 1. Diodes | | 1. Capacitors | |
|  | Answer: Option c) Capacitors |
| 76 | |  | | --- | | The circuit continuous-time feedback amplifier using capacitors & use of feedback resistor, may not be suited to amplify wideband signals because it exhibits a\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_. | | 1. low-pass transfer function | | 1. high-pass transfer function | | 1. All-pass transfer function | | 1. All-stop transfer function | |
|  | Answer: Option b) high-pass transfer function |
| 77 | |  | | --- | | In Switched-capacitor amplifier circuit, what is our assumption, before we study the circuit in two phases | | 1. that the open-loop gain of the op amp is very small | | 1. that the closed-loop gain of the op amp is very large | | 1. that the open-loop gain of the op amp is zero. | | 1. that the open-loop gain of the op amp is very large | |
|  | Answer: Option d) that the open-loop gain of the op amp is very large |
| 78 | |  | | --- | | How many switches are used in Switched-capacitor amplifier.? | | 1. one | | 1. two | | 1. three | | 1. four | |
|  | Answer: Option c) three |
| 79 | |  | | --- | | In Switched-capacitor amplifier circuit, what is our assumption, before we study the circuit in two phases | | 1. that the open-loop gain of the op amp is very small | | 1. that the closed-loop gain of the op amp is very large | | 1. that the open-loop gain of the op amp is zero. | | 1. that the open-loop gain of the op amp is very large | |
|  | Answer: Option c) that the open-loop gain of the op amp is zero. |
| 80 | |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | |  | | --- | | In switched-capacitor amplifier circuit, since VA changes from Vin0 to 0, the output voltage must change from zero to \_\_\_\_\_\_\_\_\_\_\_\_\_. | | 1. Vin0 (C1 + C2) | | 1. Vout (C1 - C2) | | 1. Vin0C1/C2 | | 1. Vin0C1\*C2 | | |  | |  | |
|  | Answer: Option c) Vin0C1/C2 |
| 81 | |  | | --- | | The measure of speed in a sampling circuit is the | | 1. Time required for the output voltage to go from zero to the maximum input level after the switch turns on | | 1. Time required for the output voltage to go from zero to the minimum input level after the switch turns on | | 1. Time required for the output voltage to go from zero to the minimum input level after the switch turns off | | 1. Time required for the input voltage to go from zero to the maximum input level after the switch turns off | |
|  | Answer: Option a) Time required for the output voltage to go from zero to the maximum input level after the switch turns on |
| 82 | |  | | --- | | Even for clock feedthrough mechanism, the circuit does not provide complete cancellation because \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_. | | 1. the gate-source overlap capacitance of NFETs is not equal to that of PFETs | | 1. the gate-drain overlap capacitance of NFETs is equal to that of PFETs | | 1. the gate-source overlap capacitance of NFETs is equal to that of PFETs | | 1. the gate-drain overlap capacitance of NFETs is not equal to that of PFETs | |
|  | Answer: Option d) the gate-drain overlap capacitance of NFETs is not equal to that of PFETs |
| 83 | |  | | --- | | It is instructive to consider the \_\_\_\_\_\_\_\_\_\_\_trade-off resulting from charge injection. | | 1. speed-precision | | 1. speed- noise | | 1. speed-power dissipation | | 1. speed-voltage swings | |
|  | Answer: Option a) speed-precision |
| 84 | Why the switches used in weighted resistor DAC are of single pole double throw (SPDT) type?  a) To connect the resistance to reference voltage  b) To connect the resistance to ground  c) To connect the resistance to either reference voltage or ground  d) To connect the resistance to output |
|  | Answer: Option c) To connect the resistance to either reference voltage or ground |
| 85 | In a D-A converter with binary weighted resistor, a desired step size can be obtained by  a) Selecting proper value of VFS  b) Selecting proper value of R  c) Selecting proper value of RF  d) Selecting proper value of Vref |
|  | Answer: Option c) Selecting proper value of RF |
| 86 | Pick out the incorrect statement “In a 3 bit weighted resistor DAC”  a) Although the op-amp is connected in inverting mode, it can also be connected in non-inverting mode  b) The op-amp simply work as a current to voltage converter  c) The polarity of the reference voltage is chosen in accordance with the input voltage  d) The op-amp simply work as a voltage to current converter |
|  | Answer: Option c) The polarity of the reference voltage is chosen in accordance with the input voltage |
| 87 | What is the disadvantage of binary weighted type DAC?  a) Require wide range of resistors  b) High operating frequency  c) High power consumption  d) Slow switching |
|  | Answer: Option a) Require wide range of resistors |
| 88 | How to overcome the limitation of binary weighted resistor type DAC?  a) Using R-2R ladder type DAC  b) Multiplying DACs  c) Using monolithic DAC  d) Using hybrid DAC |
|  | Answer: Option a) Using R-2R ladder type DAC |
| 89 | Which type of switches are not preferable for a simple weighted resistor DAC?  a) Bipolar Transistor  b) Voltage switches  c) MOSFET  d) EMOSFET |
|  | Answer: Option a) Bipolar Transistor |
| 90 | The inverted R-2R ladder can also be operated in \_\_\_\_\_\_\_\_.  a) Inverted mode  b) Current Mode  c) Voltage mode  d) Non inverted mode |
|  | Answer: Option b) Current Mode |
| 91 | Multiplying DAC uses  a) Varying reference voltage  b) Varying input voltage  c) Constant reference voltage  d) Constant input voltage |
|  | Answer: Option a) Varying reference voltage |
| 92 | Which of among the following circuit is considered to be linear?  a) Weighted Resistor type DAC  b) R-2R ladder type DAC  c) Inverter R-2R ladder DAC  d) Successive Approximation Type |
|  | Answer: Option c) Inverter R-2R ladder DAC |
| 93 | In a servo tracking A/D converter, the input voltage is greater than the DAC output signal at this condition  a) The counter count up  b) The counter count down  c) The counter back and forth  d) The counter count up and down |
|  | Answer: Option a) The counter count up |
| 94 | How many equal intervals are present in a 14-bit D-A converter?  a) 16383  b) 4095  c) 65535  d) 1023 |
|  | Answer: Option a)16383 |
| 95 | Select the specifications that implies the inverting amplifier?  a) V1 = -3v, V2 = -4v  b) V1 = -2v, V2 = 3v  c) V1 = 5v, V 2 = 15v  d) V1 = 0v, V2 = 5v |
|  | Answer: Option d) V1 = 0v, V2 = 5v |
| 96 | The closed loop voltage gain is reciprocal of  a) Voltage gain of op-amp  b) Gain of the feedback circuit  c) Open loop voltage gain  d) Current gain of op-amp |
|  | Answer: Option b) Gain of the feedback circuit |
| 97 | A standard block diagram of closed loop system composes of  a) Two blocks  b) Single block  c) Three blocks  d) Four Blocks |
|  | Answer: Option a) Two blocks |
| 98 | Name the block connected in the feedback path  a) Feedback block  b) Forward block  c) Output block  d) Summation of feedback, forward and output block |
|  | Answer: Option a) Feedback block |
| 99 | Find out the system stability when a system has three RC poles pairs  a) Attain stability at low frequency  b) Attain stability at high frequency  c) Attain instability at high frequency  d) Attain instability at low frequency |
|  | Answer: Option c) Attain instability at high frequency |
| 100 | Measure taken to increase the bandwidth of an op-amp.  a) Increase the frequency for the configuration  b) Reduce the gain of the configuration  c) Closed loop configuration is used  d) Open loop configuration is used |
|  | Answer: Option c) Closed loop configuration is used |
| 101 | Why unstable systems are considered to be impractical?  a) Input decreases with time  b) Output decreases with time  c) Output reaches fixed value  d) Output increases with time |
|  | Answer: Option d) Output increases with time |
| 102 | When does a system said to be stable?  a) Output reaches a minimum value at finite time  b) Output reaches a maximum value at any time  c) Output reaches a fixed value at finite time  d) Output reaches a fixed value at any time |
|  | Answer: Option c) Output reaches a fixed value at finite time |
| 103 | Open loop configuration is not preferred in op-amps because  a) First break frequency is too large  b) First break frequency is very small  c) Second break frequency is too large  d) Second break frequency is too small |
|  | Answer: Option b) First break frequency is very small |
| 104 | Which type of op-amp offer relatively broader open-loop bandwidth?  a) Compensated op-amp  b) Uncompensated op-amp  c) Tailored frequency response op-amp  d) Non-compensated op-amp |
|  | Answer: Option b) Uncompensated op-amp |
| 105 | . Open loop bandwidth of an op-amp extend its bandwidth from \_\_\_\_\_  a) 0Hz to fo  b) 20dB to fo  c) 3dB to fo  d) 0.704dB to fo |
|  | Answer: Option a) 0Hz to fo |
| 106 | An ideal op-amp requires infinite bandwidth because \_\_\_\_\_\_  a) Signals can be amplified without attenuation  b) Output common-mode noise voltage is zero  c) Output voltage occurs simultaneously with input voltage changes  d) Output can drive infinite number of device |
|  | Answer: Option a) Signals can be amplified without attenuation |
| 107 | Ideal op-amp has infinite voltage gain because  a) To control the output voltage  b) To obtain finite output voltage  c) To receive zero noise output voltage  d) To control the input voltage |
|  | Answer: Option b) To obtain finite output voltage |
| 108 | How does the physical characteristic of semiconductor account for the increase in frequency of op-amps?  a) Transistor values  b) Junction capacitance  c) Dopant concentration  d) Aspect Ratios of MOSFET |
|  | Answer: Option b) Junction capacitance |
| 109 | The current gain of a simple CG stage is approximately \_\_\_  a) Infinity  b) unity  c) twice  d) 0 |
|  | Answer: Option unity |
| 110 | What is the ideal output voltage of analog multiplier provided with two input signal Vx and Vy and Km is the multiplier gain ?   1. Km VxVy 2. VxVy/Km 3. 0.5KmVxVy 4. 2KmVxVy |
|  | Answer: Option a) Km VxVy |