Program: BE EXTC Engineering

Curriculum Scheme: Revised 2012

Examination: Third Year Semester VI

Course Code: ETC606 and Course Name: VLSI DESIGN

Time: 1-hour Max. Marks: 50

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Note to the students: - All the Questions are compulsory and carry equal marks.

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| Q1. | In CMOS fabrication, the photoresist layer is exposed to \_\_\_\_\_\_\_ |
| Option A: | visible light |
| Option B: | ultraviolet light |
| Option C: | infra red light |
| Option D: | fluorescent |
|  |  |
| Q2. | Few parts of photoresist layer is removed by using \_\_\_\_ |
| Option A: | acidic solution |
| Option B: | neutral solution |
| Option C: | pure water |
| Option D: | diluted water |
|  |  |
| Q3. | What is Lithography? |
| Option A: | Process used to transfer a pattern to a layer on the chip |
| Option B: | Process used to develop an oxidation layer on the chip |
| Option C: | Process used to develop a metal layer on the chip |
| Option D: | Process used to produce the chip |
|  |  |
| Q4. | Silicon oxide is patterned on a substrate using \_\_\_\_\_\_\_ |
| Option A: | Physical lithography |
| Option B: | Photolithography |
| Option C: | Chemical lithography |
| Option D: | Mechanical lithography |
|  |  |
| Q5. | Which among the following devices is the most suited for high frequency applications? |
| Option A: | BJT |
| Option B: | IGBT |
| Option C: | MSFET |
| Option D: | SCR |
|  |  |
| Q6. | Consider an ideal MOSFET. If Vgs = 0V, then Id = ? |
| Option A: | 0V |
| Option B: | Maximim |
| Option C: | Id(on) |
| Option D: | Idd |
|  |  |
| Q7. | The basic advantage of the CMOS technology is that |
| Option A: | It is easily available |
| Option B: | It has small size |
| Option C: | It has lower power consumption |
| Option D: | It has better switching capabilities |
|  |  |
| Q8. | If n-transistor conducts and has large voltage between source and drain, then it is said to be in \_\_\_\_\_ region. |
| Option A: | linear |
| Option B: | saturation |
| Option C: | non saturation |
| Option D: | cut-off |
|  |  |
| Q9. | If p-transistor is conducting and has small voltage between source and drain, then it is said to work in \_\_\_\_\_\_\_\_ |
| Option A: | linear region |
| Option B: | saturation region |
| Option C: | non saturation resistive region |
| Option D: | cut-off region |
|  |  |
| Q10. | In VLSI design, which process deals with the determination of resistance & capacitance of interconnections? |
| Option A: | Floorplanning |
| Option B: | Placement & Routing |
| Option C: | Testing |
| Option D: | Extraction |
|  |  |
| Q11. | Pass transistor can be driven through \_\_\_\_\_ pass transistors |
| Option A: | 1 |
| Option B: | No |
| Option C: | More |
| Option D: | 2 |
|  |  |
| Q12. | Switch logic approach is fast for |
| Option A: | large arrays |
| Option B: | small arrays |
| Option C: | very large arrays |
| Option D: | not at all fast for any type |
|  |  |
| Q13. | Switch logic is designed using |
| Option A: | conductors |
| Option B: | silicon plates |
| Option C: | resistors |
| Option D: | complementary switches |
|  |  |
| Q14. | Pass transistors require lower switching energy to charge up a node, due to |
| Option A: | increase voltage swing |
| Option B: | reduces current swing |
| Option C: | reduces voltage swing |
| Option D: | increase current swing |
|  |  |
| Q15. | Why is SRAM more preferably in non-volatile memory? |
| Option A: | low-cost |
| Option B: | high-cost |
| Option C: | low power consumption |
| Option D: | transistor as a storage element |
|  |  |
| Q16. | Which of the following ahs refreshes control mechanism? |
| Option A: | DRAM |
| Option B: | SRAM |
| Option C: | Battery backed-up SRAM |
| Option D: | Pseudo-static RAM |
|  |  |
| Q17. | Which type of storage element of SRAM is very fast in accessing data but consumes lots of power? |
| Option A: | CMOS |
| Option B: | TTL |
| Option C: | NAND |
| Option D: | NOR |
|  |  |
| Q18. | What is approximate data access time of SRAM? |
| Option A: | 10ns |
| Option B: | 2ns |
| Option C: | 4ns |
| Option D: | 60ns |
|  |  |
| Q19. | Fast-look-ahead carry circuits found in most 4-bit full-adder circuits which \_\_\_\_\_\_\_\_\_\_\_ |
| Option A: | Increase ripple delay |
| Option B: | Add a 1 to complemented inputs |
| Option C: | Reduce propagation delay |
| Option D: | Determine sign and magnitude |
|  |  |
| Q20. | What distinguishes the look-ahead-carry adder? |
| Option A: | It is faster than a ripple-carry adder |
| Option B: | It is slower than the ripple-carry adder |
| Option C: | It is easier to implement logically than a full adder |
| Option D: | It requires advance knowledge of the final answer |
|  |  |
| Q21. | What is one disadvantage of the ripple-carry adder? |
| Option A: | More stages are required to a full adder |
| Option B: | It is slow due to propagation time |
| Option C: | The interconnections are more complex |
| Option D: | More stages are required to a full and Half adder |
|  |  |
| Q22. | Clocked sequential circuits are |
| Option A: | four phase non overlapping clock |
| Option B: | four phase overlapping clock |
| Option C: | two phase non overlapping clock |
| Option D: | two phase overlapping clock |
|  |  |
| Q23. | \_\_\_\_\_\_\_\_\_\_\_ is used to drive high capacitance load. |
| Option A: | single polar capability |
| Option B: | bipolar capability |
| Option C: | tripolar capability |
| Option D: | nullpolar capability |
|  |  |
| Q24. | Inverting dynamic register element consists of \_\_\_\_\_\_\_\_\_\_ transistors for nMOS and \_\_\_\_\_\_\_\_\_ for CMOS. |
| Option A: | two, three |
| Option B: | three, four |
| Option C: | three, two |
| Option D: | four, three |
|  |  |
| Q25. | Non inverting dynamic register storage cell consists of \_\_\_\_\_\_\_\_\_ transistors for nMOS and \_\_\_\_\_\_\_\_\_ for CMOS. |
| Option A: | six, eight |
| Option B: | eight, six |
| Option C: | five, six |
| Option D: | six, five |