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RAM MEMORY DESIGN IN VERILOG USING FPGA

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Abstract−There are many systems which use RAM as its primary memory for example spacecraft, our home computer etc. Energy efficient RAM is even more important in outer space exploration as the power source is very limited and the environmental condition is extreme. Energy efficiency is not only based on the architecture of the system but also on the environmental condition. For that reason, low power RAM will increase the performance of the system even in extreme conditions. In this project, we are advancing towards a design of RAM that will consume less power even in extreme conditions. Four contemporary FPGAs are used for implementation of our RAM design and we find the least power consumer among these four FPGAs architectures.

I. INTRODUCTION

RAM allows your computer to perform many of its everyday tasks, such as loading applications, browsing the internet, editing a spreadsheet, or experiencing the latest game. Memory also allows you to switch quickly among these tasks, remembering where you are in one task when you switch to another task.

Random-access memory (RAM) is a form of computer memory that can be read and changed in any order, typically used to store working ((data and machine code. A random-access memory device allows data items to be ((read or written in almost the same amount of time irrespective of the physical location of data inside the memory, in contrast with other direct-access data storage media (such as hard disks, CD-RWs, DVD-RWs and the older magnetic tapes and drum memory), where the time required to read and write data items varies significantly depending on their physical locations on the recording medium, due to mechanical limitations such as media rotation speeds and arm movement.

RAM contains multiplexing and demultiplexing circuitry, to connect the data lines to the addressed storage for reading or writing the entry. Usually more than one bit of storage is accessed by the same address, and RAM devices often have multiple data lines and are said to be "8-bit" or "16-bit", etc. devics.

In this project we have designed a digital RAM on FPGA designed from FPGA based are easier to program and can be reconfigured anytime without changing the whole machine design. Essentially, an FPGA is a hardware circuit that a user can program to carry out one or more logical operations. FPGAs are programmable silicon chips with a collection of programmable logic blocks surrounded by Input/Output blocks that are put together through programmable interconnect resources to become any kind of digital circuit or system. To solve this problem, the requested algorithm needs to be implemented in FPGA using combinational or sequential logic to ensure a response time that is always the same and under milliseconds.

II DESIGN SYSTEM

II.1. BLOCK DIAGRAM

RAM is a combinational circuit of multiplexer and decoder that has maximum of 2n address bit, ‘n’ selection

lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines. Since, there are ‘n’ selection lines, there will be 2n possible combinations of zeros and ones.

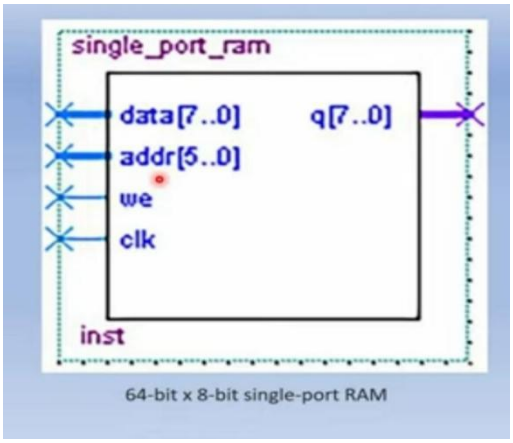

Figure 1. 64-bit X 8-bit single port RAM

Port Name	Type	Description
data[7:0]	Input	8-bit data input
addr[5:0]	Input	6-bit address input
we	Input	Write enable input
clk	Input	Clock input

Table 1.1 Single-port RAM Description in tabular format

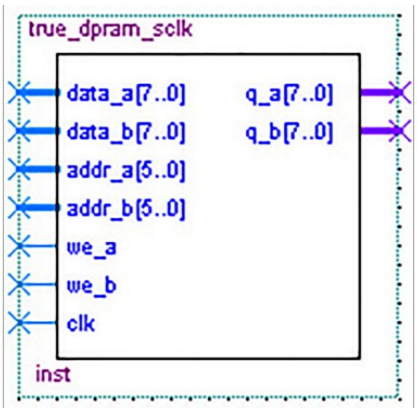

Figure 2. 64-bit X 8-bit dual port RAM

Port Name	Type	Description
dataa[7:0], datab[7:0]	Input	8 bit data inputs of port A and port B
addr_a[5:0], addr_b[5:0]	Input	6 bit address inputs of port A and port B
we_a, we_b	Input	Write enable inputs of port A and port B
clk	Input	Clock input
q_a[7:0], q_b[7:0]	Output	8 bit data outputs of port A and port B

Table 2.1 Dual-port RAM Description in tabular format

II.2 DESIGN OF CIRCUIT DIAGRAM

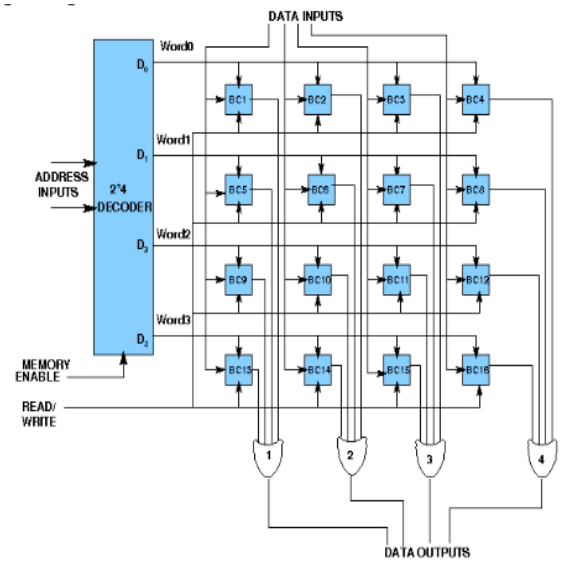

Figure 3. Logical Circuit Diagram of 4X4 RAM

The logical construction of a small RAM 4X3 is shown below. It consists of 4 words of 3 bits each and has a total of 12 binary cells. A memory with 4 words needs two address lines. The two address inputs go through a 2*4 decoder to select one of the four words. The decoder is enabled with the memory enable input. When the memory enable is 0, all outputs of the decoder are 0 and none of the memory words are selected. With the memory enable at 1, one of the four words is selected, dictated by the value in the two address lines.

III. WORKING

RAM is capable to perform two operations like as Read and Write. Read means signal transferring out, and Write means signal transferring in. RAM permits one of these control signals, internal circuit that is embedded into inside memory which are delivered the required function, which are expected from the user side. Supply binary address of the required word inside the address lines. Supply the data bits which are must be hold into memory internal of data input lines.

IV. SOFTWARE USED

To program FPGA in VERILOG language we have used the EDA Playground. EDA Playground is a free web application that allows users to edit, simulate (and view waveforms), synthesize, and share their HDL code. Its goal is to accelerate the learning of design and testbench development with easier code sharing and with simpler access to simulators and librariesIt supports several HDLs such as System Verilog, VHDL, MyHDL, and Migen. Verification engineers may play with several libraries and methodologies, such as UVM, OVL, SVUnit, etc.

EDA for electronics has rapidly increased in importance with the continuous scaling of semiconductor technology. Some users are foundry operators, who operate the semiconductor fabrication facilities ("fabs") and additional individuals responsible for utilising the technology design-service companies who use EDA software to evaluate an incoming design for manufacturing readiness.

There are also other softwares available like ModelSim is a multi-language environment by Mentor Graphics, for simulation of hardware description languages such as VHDL, Verilog and SystemC, and includes a built-in C debugger. ModelSim can be used independently, or in conjunction with Intel Quartus Prime, PSIM, Xilinx ISE or Xilinx Vivado.

The HDL simulator is also crucial because the process of compiling a given hardware description into an FPGA board and programming the board itself, can be very time-consuming, even for a simple program. The simulator allows you to thoroughly verify the algorithm you want to implement into an FPGA board**.**

V. RESULTS

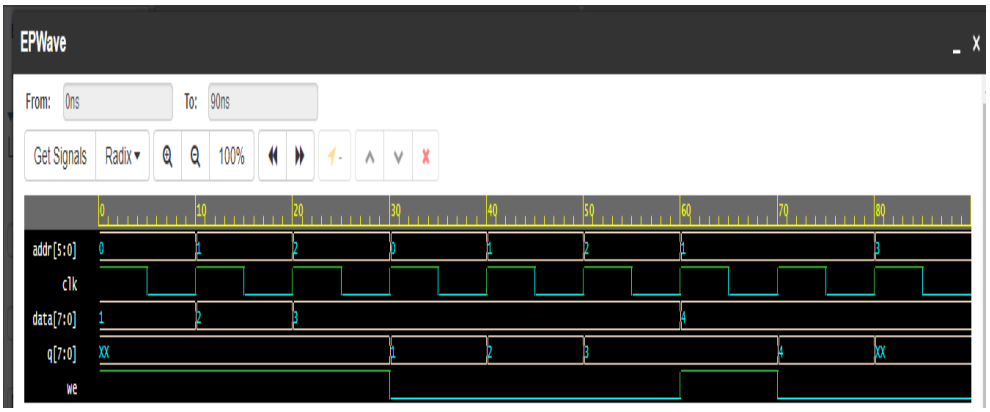

Figure 4. Waveform of read & write of Single Port RAM

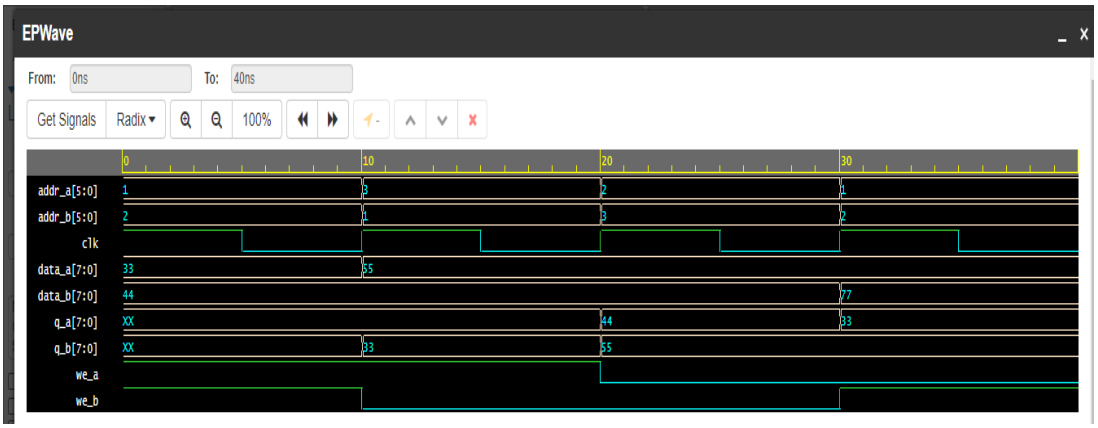

Figure 5. Waveform of read & write of Dual Port RAM

VI. CONCLUSION

This project describes a 64-bit X 8-bit single-port RAM and dual-port RAM design with common read and write addresses in Verilog HDL. Synthesis tools are able to detect single-port RAM designs in the HDL code and automatically infer either the altsyncram or the altdpram megafunctions, depending on the architecture of the target device. The circuit implemented in FPGA in much faster and efficient than general CPU's. Such a real-time system implemented in FPGA can be modified and moved into manufacturing once it is ready.

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